**Amendment to the Claims:**

1. (currently amended) A non-volatile memory cell comprising:

a control gate pattern disposed over a semiconductor substrate and comprising a tunnel insulation pattern, a trap insulation pattern, a blocking insulation pattern and a control gate electrode, which are stacked;

a selection gate electrode disposed over the semiconductor substrate at one side and extending over substantially the entire top portion of the control gate pattern;

a gate insulation pattern interposed between the selection gate electrode and the semiconductor substrate, and between the selection gate electrode and the control gate pattern, wherein the gate insulation pattern covers the entire sidewall of the selection gate electrode proximal to the control gate pattern; and

a cell channel region comprising a first channel region defined in the semiconductor substrate under the control gate pattern and a second channel region defined in the semiconductor substrate under the selection gate electrode~~; and~~

~~drain/source regions formed in the semiconductor substrate at respective sides of the cell channel region, the drain region being in contact with the first channel region and the source region being in contact with the second channel region~~.

2. (original) The non-volatile memory cell according to claim 1, wherein the tunnel insulation pattern is formed of at least one selected from the group consisting of silicon oxide and silicon oxynitride.

3. (original) The non-volatile memory cell according to claim 1, wherein the trap insulation pattern is formed of at least one selected from the group consisting of silicon nitride, polysilicon dots and nitride dots.

4. (previously presented) The non-volatile memory cell according to claim 1, wherein the selection gate electrode covers one sidewall and the top surface of the control gate electrode and is self-aligned to the other sidewall of the control gate electrode.

5. (original) The non-volatile memory cell according to claim 1, wherein the thickness of the gate insulation pattern is less than the sum of the thickness of the tunnel insulation pattern, the trap insulation pattern and the blocking insulation pattern.

6. (canceled)

7. (currently amended) The non-volatile memory cell according to claim ~~6~~1, further comprising a metal silicide layer formed over a predetermined region of a sidewall of the selection gate electrode, an exposed sidewall of the control gate electrode and a surface of the drain/source regions.

8. (previously presented) A non-volatile memory cell comprising:

a first control gate pattern and a second control gate pattern disposed in parallel over a semiconductor substrate, each of the first and second control gate patterns comprising a tunnel insulation pattern, a trap insulation pattern, a blocking insulation pattern and a control gate electrode, which are stacked sequentially;

a first selection gate electrode disposed, in parallel to the first control gate pattern, over the semiconductor substrate at one side and extending over substantially the entire top portion of the first control gate pattern;

a second selection gate electrode disposed, in parallel to the second control gate pattern, over the semiconductor substrate at one side and extending over substantially the entire top portion of the second control gate pattern;

a first gate insulation pattern interposed between the first selection gate electrode and the semiconductor substrate, and between the first selection gate electrode and the first control gate pattern;

a second gate insulation pattern interposed between the second selection gate electrode and the semiconductor substrate, and between the second selection gate electrode and the second control gate pattern;

a first cell channel region comprising a first channel region defined in the semiconductor substrate under the first control gate pattern and a second channel region defined in the semiconductor substrate under the first selection gate electrode; and

a second cell channel region comprising a first channel region

defined in the semiconductor substrate under the second control gate pattern and a second channel region defined in the semiconductor substrate under the second selection gate electrode,

wherein the first and second selection gate electrodes are disposed symmetrically over the substrate.

9. (previously presented) The non-volatile memory cell according to claim 8, wherein the tunnel insulation patterns are formed of at least one compound selected from the group consisting of silicon oxide and silicon oxynitride.

10. (previously presented) The non-volatile memory cell according to claim 8, wherein the trap insulation patterns are formed of at least one compound selected from the group consisting of silicon nitride, polysilicon dots, and nitride dots.

11. (previously presented) The non-volatile memory cell according to claim 8, wherein the first selection gate electrode covers one sidewall and the top surface of the first control gate electrode is self-aligned to the other sidewall of the first control gate electrode, and the second selection gate electrode covers one sidewall and the top surface of the second control gate electrode and is self-aligned to the other sidewall of the second control gate electrode.

12. (original) The non-volatile memory cell according to claim 8, wherein the selection gate electrodes are disposed between the control gate patterns.

13. (original) The non-volatile memory cell according to claim 12, further comprising: a first drain region in contact with the first channel region of the first cell channel region; a second drain region in contact with the first channel region of the second cell channel region; and a source region in contact with the second channel region of the first cell channel region and the second channel region of the second cell channel region.

14. (original) The non-volatile memory cell according to claim 8; wherein the control gate patterns are disposed between the selection gate electrodes.

15. (original) The non-volatile memory cell according to claim 14, further comprising: a first source region in contact with the second channel region of the first cell channel region; a second source region in contact with the second channel region of the second cell channel region; and a drain region in contact with the first channel region of the first cell channel region and the first channel region of the second cell channel region.

16. (original) The non-volatile memory cell according to claim 9, wherein the thickness of each gate insulation pattern is less than the total thickness of the tunnel insulation pattern, the trap insulation pattern and the blocking insulation pattern.

17.-35. (canceled)

36. (new) The non-volatile memory cell according to claim 1, wherein drain/source regions formed in the semiconductor substrate at respective sides of the cell channel region, the drain region being in contact with the first channel region and the source region being in contact with the second channel region.